UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,021	07/31/2003	Inderiit Singh	NVIDP235/P000846	4737

28875 7590 07/18/2008

Zilka-Kotab, PC
P.O. BOX 721120
SAN JOSE, CA 95172-1120

EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
07/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte INDERIIT SINGH, HOWARD LEE MARKS,
and JOSEPH DAVID GARCO

Appeal 2008-1137
Application 10/633,021
Technology Center 2800

Decided: July 18, 2008

Before ANITA PELLMAN GROSS, MAHSHID D. SAADAT,
and KEVIN F. TURNER, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a final rejection of claims 1, 2, 4-14, 16-18, 24, 26, 27, 29, and 30, which are all of the claims pending in this application, as claims 3, 15, 19-23, 25, and 28 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

Appellants' invention relates to placement of metal layers and a bond pad, at least partially, above the active circuits in an integrated circuit (Spec. 3).

Claim 1 is representative of the claims on appeal and reads as follows:

1. An integrated circuit, comprising:

an active circuit;

a metal layer disposed, at least partially, above the active circuit; and

a bond pad disposed, at least partially, above the metal layer;

wherein the metal layer defines a frame;

wherein the metal layer is disposed, at least partially, directly above the active circuit;

wherein the frame ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process;

wherein the active circuit includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad, and the frame ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Tanaka	US 6,100,589	Aug. 8, 2000
Suzuki	US 6,707,156 B2	Mar. 16, 2004 (filed Jan. 28, 2003)

Appellants' Admitted Prior Art (AAPA), as depicted in Figures 1-2.

Claims 1, 2, 4-14, 16-18, 24, 26, 27, 29, and 30 stand rejected under the first paragraph of 35 U.S.C. § 112 as containing subject matter which was not described in the Specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Claims 1, 4-14, 16, 18, 24, 26, 27, 29, and 30 stand rejected under 35 U.S.C. § 103(a) based upon the teachings of Suzuki and Tanaka.

Claims 2 and 17 stand rejected under 35 U.S.C. § 103(a) based upon the teachings of Suzuki and Tanaka in view of AAPA.

Rather than reiterate the opposing arguments, reference is made to the Briefs and the Answer for the respective positions of Appellants and the Examiner. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

We affirm.[1]

ISSUES

The first issue on appeal turns on whether under the first paragraph of 35 U.S.C. § 112, with respect to all the appealed claims, the Specification, as originally filed, supports the claimed "an entirety of at least one of the transistors is disposed directly below the bond pad."

---

[1] Our decision, in most parts, is the same as the panel decision of Mar. 26, 2008, in the related appeal 2007-4511, filed in Application 10/633,004, which involved similar issues and included identical arguments.

The second issue is whether under 35 U.S.C. § 103, with respect to appealed claims 1, 4-14, 16, 18, 24, 26, 27, 29, and 30, the combination of Suzuki and Tanaka, as proposed by the Examiner, teaches or suggests the claimed subject matter.

The third issue is whether under 35 U.S.C § 103(a) with respect to appealed claims 2 and 17, one of ordinary skill in the art at the time of the invention would have found it obvious to modify Suzuki and Tanaka based on AAPA to render the claimed invention unpatentable.

PRINCIPLES OF LAW

Written Description

"The purpose of the written description requirement is to prevent an applicant from later asserting that he invented that which he did not; the applicant for a patent is therefore required 'to recount his invention in such detail that his future claims can be determined to be encompassed within his original creation.'" *Amgen Inc. v. Hoechst Marion Roussel Inc.*, 314 F.3d 1313, 1330 (Fed. Cir. 2003) (citing *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1561 (Fed. Cir. 1991)). While there is no requirement that the claimed invention be described in the identical wording that was used in the Specification, there must be sufficient disclosure to show one of skill in this art that the inventor "invented what is claimed." *See Union Oil Co. of California v. Atlantic Richfield Co.*, 208 F.3d 989, 997 (Fed. Cir. 2000) (citing *In re Gosteli*, 872 F.2d 1008, 1012 (Fed. Cir. 1989)).

The written description must be of sufficient detail to show possession of the full scope of the invention. *Pandrol USA LP v. Airboss Railway Products Inc.*, 424 F.3d 1161, 1165 (Fed. Cir. 2005).

Obviousness

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). "[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

In identifying a reason that would have prompted a person of ordinary skill in the relevant field to combine the prior art teachings, the Examiner must show some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *KSR Int'l. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007). "[T]here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (citing *In re Lee*, 277 F.3d 1338, 1343-46 (Fed. Cir. 2002); *In re Rouffet*, 149 F.3d 1350, 1355-59 (Fed. Cir. 1998)).

Further, a rejection based on section 103 must rest upon a factual basis rather than conjecture, or speculation. "Where the legal conclusion [of obviousness] is not supported by the facts it cannot stand." *In re Warner*, 379 F.2d 1011, 1017 (CCPA 1967). *See also In re Kahn*, 441 F.3d at 988 (Fed. Cir. 2006).

ANALYSIS

35 U.S.C. § 112 Rejection of the claims

With respect to the written description issue, the Examiner asserts that disposing an entirety of at least one of the transistors directly below the bond pad, as recited in independent claims 1 and 16-18, has no support in the originally filed Specification (Ans. 3). The Examiner acknowledges that Appellants' disclosure specifies that the bond pad 306 is disposed above the core 302 and/or above any part of the active circuit 308, while the active circuit 308 may include a plurality of transistors (Ans. 10). However, the Examiner argues that the disclosed placement of the bond pad 306 does not necessarily place an entirety of at least one of the transistors directly below the bond pad (*id.*).

Appellants contend that by virtue of the disclosure in the originally filed application, on page 3, lines 10-11, and the original claim 17, and since the active circuit and the core may include a plurality of transistors, while the bond pads may be disposed above the core and other parts of the active circuit, the disclosure meets the written description requirement (App. Br. 11). Appellants conclude that since the bond pads 306 may be disposed above the core 302 and any other part of the active circuit 308, and the core 302 of the active circuit 308 includes a plurality of transistors, the Specification does disclose "an entirety of at least one of the transistors is disposed directly below the bond pad," as claimed (App. Br. 11; Reply Br. 2-3).

Upon a review of the evidence of record and the arguments presented by Appellants and the Examiner, we agree with Appellants. The disclosure that the bond pads are disposed above the core, and/or any other part of the

active circuit (Spec. 7:15-17), remains uncontested. Such an arrangement clearly indicates the placement of the bond pads over any part of the active circuit which includes both the core and the peripheral I/O bus or any devices formed in the integrated circuit. As argued by Appellants (Reply Br. 3), even if the exact wording is not used to explicitly disclose the disputed claim limitation, there is sufficient disclosure that shows one of ordinary skill in the art that Appellants invented and disclosed the specific claimed placement of the bond pads.

Thus, contrary to the Examiner's assertion, upon reading Appellants' disclosure, a person of ordinary skill in the art would be led to the conclusion that an entirety of at least one of the transistors would be able to be disposed directly below the bond pad, according to the claimed invention.

As there is sufficient disclosure in Appellants' Specification with respect to the placement of the bond pads, we find that the specified placement of the bond pads above the core and any other part of the active circuit represents a disclosed feature within the scope of the claimed and disclosed invention representing no new matter. Accordingly, we do not sustain the rejection of claims 1, 2, 4-14, 16-18, 24, 26, 27, 29, and 30 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the Specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

35 U.S.C. § 103 Rejection of Claims 1, 4-14, 16, 18, 24, 26, 27, 29, and 30

Appellants contend that Tanaka and Suzuki address different problems of arranging bond pads and cannot be combined since Suzuki does not even mention bonding or any problems associated with the bonding-related damages to the active circuit (App. Br. 12; Reply Br. 4-5). The Examiner responds by relying on Figure 1 of Suzuki and stating that the bond pad is shown over a stack of metal layers and disposed above an entirety of at least one transistor (Ans. 11). The Examiner further points out that the bond pad disclosed in Suzuki must certainly be used for connection to a bond wire (*id.*).

We agree with the Examiner's assessment of the structure depicted in Figure 1 of Suzuki where active region 13 and its neighboring regions correspond to an entirety of at least one transistor that is disposed directly below the bond pad, as represented by metal layer M11L. Suzuki further discloses that the metal layer M11L is a wiring layer or a pad (col. 4, ll. 58-67). Therefore, Suzuki discloses a bond pad, which is used for connection to the wiring, to be positioned over an entirety of at least a transistor in the active circuit area.

With respect to the recognition of any problems associated with bonding to the pad, we also agree with the Examiner (Ans. 11) that Suzuki describes how the dielectric layers between the metal layers are formed to reduce the stress induced by the stack (col. 6, ll. 16-31). Therefore, one of ordinary skill in the art would have concluded that some kind of stress is induced in the layers below the bond pad even before any bonding is performed.

Turning now to Tanaka, we note that Appellants take a similar position that the reference does not address the problem of bonding-related damage to the active circuit (App. Br. 12; Reply Br. 5-7). The Examiner argues that Tanaka does address the stress problem in the dielectric layers by forming the frame metal layers in order to prevent formation of cracks in the insulating interlayers in the event force, such as that used for bonding, is applied to the bond pads (Ans. 11).

We also agree with the Examiner's analysis of Tanaka (Ans. 11) in suggesting the use of frame metal layers 200, 500, and 502 to reduce stress and to prevent crack propagation. Tanaka specifically illustrates in Figures 21A and 21B the formation of stress-induced cracks in the dielectric layers between metal layers and how using frame metal layer configuration and insulating props in the openings strengthens the dielectric to resist cracking (col. 7, l. 47 through col. 8, l. 48).

We also find Appellants' argument (Reply Br. 9) that Tanaka prevents cracks in the dielectric layer by using a prop of the insulating interlayer film to be unpersuasive. Appellants apparently take the "prop" 130 shown in Figure 21B to be a separate and different piece from the dielectric interlayer. Tanaka actually discloses that by using a frame metal layer, the dielectric layer is formed in a continuous form through the opening in the opening of the frame and connecting the two dielectric layers 150 and 160 (col. 8, ll. 5-8). What Tanaka calls "prop" is this solid area of continuous dielectric mass, and not a different layer other than the interlayer dielectric material. Therefore, the solid portion 130 connecting the dielectric layers forms a much stronger block to support the metal layers even if force is applied during wire-bonding (col. 7, ll. 52-54).

We further agree with the Examiner's rationale for combining Tanaka with Suzuki to further improve the reliability of the dielectric interlayers formed between the metal layer stack disclosed in Suzuki. Contrary to Appellants' assertion related to the use of a gradual change in the dielectric constant in Suzuki (Reply Br. 7-8), as discussed above, one of ordinary skill in the art, knowing about Tanaka, would have used frame metal layers in the structure of Suzuki to further reduce stress on the layers of dielectric as well as any other layer or active device that is disposed under the metal layer stack. Therefore, other approaches Suzuki uses to improve the stress problem in the dielectric layers notwithstanding and according to *KSR*, applying the teachings of Tanaka would have produced only predictable results and improved the device of Suzuki by protecting the lower layers from stress, both from dielectric layers having different constants and the pressure applied during wire-bonding to the bond pad of Suzuki.

Thus, based on our analysis above, we find that one of ordinary skill in the art would have found the Examiner's reliance on the combination of Suzuki and Tanaka to be reasonable in rendering the subject matter of claim 1 obvious. Therefore, to the extent claimed, the combination of Suzuki and Tanaka suggests the subject matter recited in representative claim 1, as well as claims 4-14, 16, 18, 24, 26, 27, 29, and 30, argued together with claim 1 as one group (App. Br. 11).

35 U.S.C. § 103 Rejection of Claims 2 and 17

With respect to claim 2, Appellants argue the patentability of the claim based on the same contentions presented with respect to claim 1 (App. Br. 14; Reply Br. 12), which are discussed above and found to be

unpersuasive. However, with respect to claim 17, Appellants argue that the AAPA Figure 2 does not show an active circuit including an input/output bus and metal layers, at least partially, under the active circuit (App. Br. 15; Reply Br. 12-13). We agree with the Examiner (Ans. 12) that the AAPA Figures 1 and 2 show that a plurality of metal layers are, at least partially, under the active circuit and around a periphery. Although the Examiner's position is stated with minimal details, it is implied that the claim limitation of "under" has been interpreted as "at a lower level" by the Examiner. We find such interpretation to be reasonable as the claim does not require the metal layers to be directly below or under the active area.

In view of the above discussions, we find that the Examiner has properly relied on the disclosure of Suzuki and Tanaka in combination with AAPA to render obvious the subject matter of claims 2 and 17. Therefore, to the extent claimed, we find that the combination of Suzuki and Tanaka with AAPA suggests the subject matter recited in claims 2 and 17.

DECISION

The decision of the Examiner with respect to the 35 U.S.C. § 103 rejections of the claims is affirmed, but is reversed with respect to the rejection under 35 U.S.C. § 112.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

eld

ZILKA-KOTAB, P.C.
P.O. BOX 721120
SAN JOSE, CA 95172-1120